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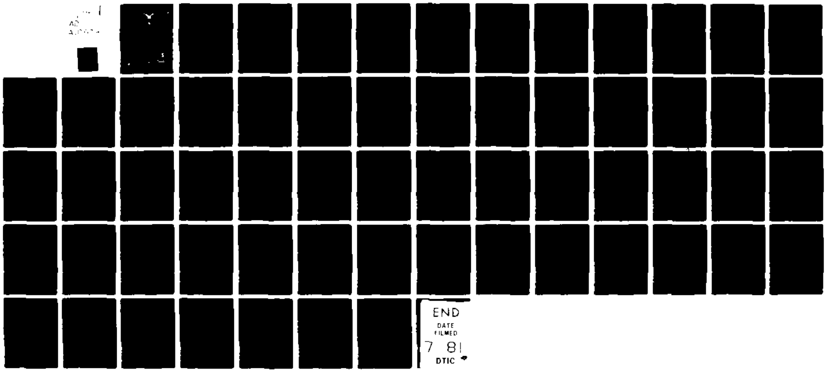

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PROGRAMMED CONTROL OF OPTICAL

GRATING SCALES FOR VISUAL RESEARCH,

THESIS

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Captain USAF



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GE/EE/80D-29

# PROGRAMMED CONTROL OF OPTICAL GRATING SCALES FOR VISUAL RESEARCH

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by

Kenneth L. Martindale, BSEE
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Graduate Electrical Engineering

December 1980

# Preface

The Aerospace Medical Research Laboratory (AMRL) is actively involved in research aimed at understanding the operation of the human visual system. Nearly all aspects of this research revolve around some type of display device. The brightness and contrast parameters of these display devices must be tightly controlled to produce valid results. This thesis describes a control device which automatically sets these parameters to the levels desired by the experimenter.

I would like to thank AMRL for their financial support, and Capt Arthur Ginsburg for his help in formulating the problem and developing criteria for its solution. Also, I would like to offer a special thanks to Dr. Matthew Kabrisky who acted as my advisor, tutor, and sounding board during this project.

Kenneth L. Martindale

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## Abstract

This report documents the design of a microprocessor based device which controls the brightness and contrast levels of video signals. The device will be used by scientists in vision research to control laboratory monitors.

Contrast control in a standard CRT monitor is obtained through the use of a commercial video chip linear circuit, and brightness control via a straight forward transistor amplifier. The transistor is inserted into the monitor's existing manual control circuit. The linear circuit and transistor are regulated by the microprocessor through digital-to-analog converters.

A feedback network reports the actual brightness and contrast produced on the monitor's screen. This network is comprised of a 1024 element photo diode array and an analog-to-digital converter. The photo diode array measures the luminance directly off the monitor and the analog-to-digital converter digitizes the information for use by the microprocessor.

The report also contains the results of an investigation into the use of digitally generated video and color monitors for vision research. The investigation found systems capable of producing 1/2 of 1% contrast, 20 cycles per degree resolution for a subject 2-1/2 feet away, and a virtually limitless range of color.

# I Introduction

## Background

Scientists of the Aerospace Medical Research Laboratory (AMRL) conduct many experiments to try to understand and quantify the human visual system. The Air Force Institute of Technology (AFIT) has also spent much time and effort in visual studies. Work has been done on the modulation transfer function of the eye (Ref 1), the center-surround receptive field model of the human visual system (Ref 2,3), and two dimensional sine wave luminance gratings (Ref 4,5). While this is only a partial list of investigative reports, all were concerned with measurements of spatial frequency resolution. They all had two common variables that had to be tightly controlled - contrast and brightness. To obtain valid results for many of the experiments involving spatial frequency resolution of the eye, contrast and brightness must be accurately known or readily measurable to within some known tolerance. Failure to control either of these parameters adequately can result in inconsistent, incorrect, and inconclusive data.

Data are usually obtained from some type of psychophysical experiment where a subject's response is measured or observed consequent to an appropriate visual stimulus. The experimenter then tries to describe the visual system via the stimulus-response relationships. AMRL is trying to quantify the spatial frequency detection capabilities of the eye as a new clinical measure of the visual system. The standard test or measure of vision has long been based on the Snellen eye chart. However, this test deals only with visual acuity. AMRL feels the eye needs a broader evaluation than visual acuity: hence their interest in spatial frequency detection or resolution.

Spatial frequency experiments use several types of stimuli, but the most common is the sinusoidal grating pattern. The contrast of this pattern is defined in terms of its maximum and minimum luminance levels:

$$\text{contrast} = \frac{L_{max} - L_{min}}{L_{max} + L_{min}} \qquad (1)$$

The average luminance is considered the brightness. Therefore, contrast and brightness ($L_{avg}$) can be related by normalizing the luminance levels of Equation (1):

$$\text{contrast} = \frac{L_{avg} + \Delta - (L_{avg} - \Delta)}{L_{avg} + \Delta + (L_{avg} - \Delta)}$$

$$= \frac{\Delta}{L_{avg}} \qquad (2)$$

where $\Delta$ = Amplitude of the sine wave

Figure 1 depicts the relationship.

AMRL currently validates its experiments by constant manual measurement and readjustment of contrast and brightness levels on the visual display device being used. This

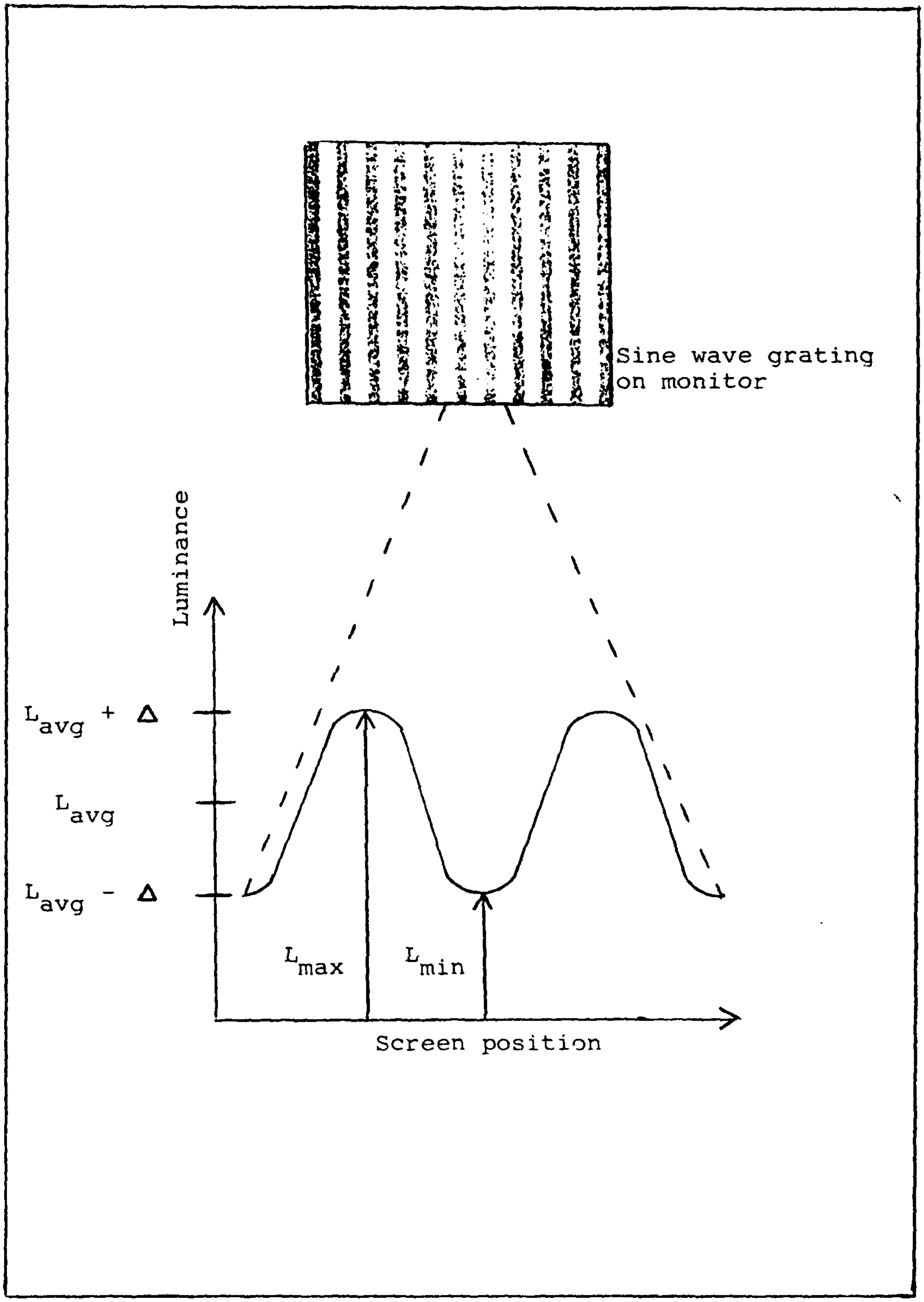



Fig. 1  Sine Wave and Luminance Relationship

can be very time consuming and a disruptive influence on subjects when the experimenter has to remeasure when changing brightness and contrast levels in a series of experiments. One typical visual display device used by AMRL is a small 9 inch RCA black and white monitor (model TC 1209). This monitor displays sine wave gratings that are generated by a microprocessing device built by Optronix.

## Problem

AMRL would like to have a device that would automatically set brightness and contrast for its RCA 9 inch monitor. The device should be able to verify the correctness of the levels requested. The objective of this thesis is to design such a device, identify the components needed, and construct the device.

## Sequence of Presentation

Section II will describe the design problems and considerations used in developing the device. Section III will quantify the requirements of the design to enable component selection. Section IV will document the intergration of the components and problems incurred in construction. Finally, Section V will present conclusions and recommendations for future work or expansion.

# II Design

## Video Circuits

The first thoughts in the design of this device involved determining at what point to control the video signal. The initial thought was to control the signal at its source - the Optronix. By altering the Optronix's programs to include a calibration routine for brightness and contrast, the video signal could be generated with the desired levels at the beginning. However, AMRL was not sure if the Optronix would become its principal source of video in the future. The desire to have a more universal device, not married to any particular video generation source, was thought more appropriate.

This desire led to two more ideas: one manipulating the contrast and brightness controls of the monitor, the other intercepting the video signal enroute to the monitor. The first option destroys the desire for universatility by directly modifying the monitor. However, the second alters neither the source (the Optronix) nor the receptor (the monitor).

The interception alternative involves receiving the Optronix video as an input, modifying the brightness and contrast, and then passing the signal on to the monitor. Figure 2 is a block diagram of this alternative.

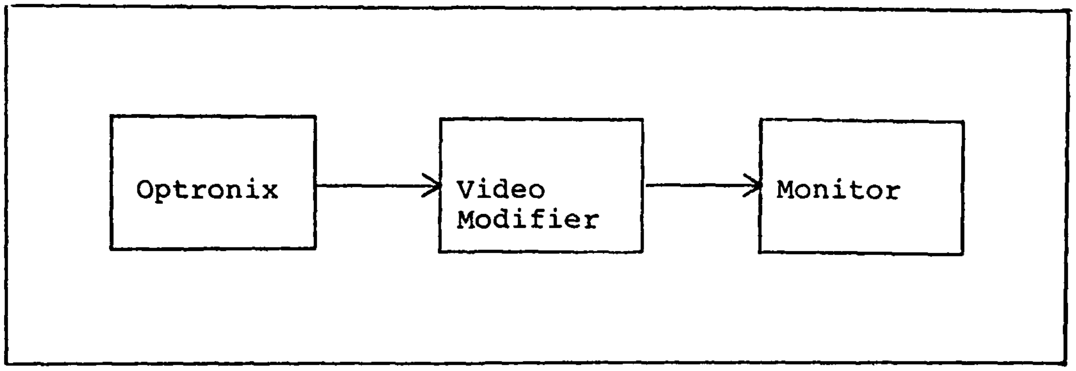



Fig. 2 Video Interception Alternative

One way to build this video modifier is to use a "jungle circuit", such as the Sylvania ECG 731, which strips sync pulses off the composite video signals. The separated sync signals can then be used to strip the sync from the video by passing the composite video through a hi-slew-rate operational amplifier (op amp) gated off by the sync pulses. By passing this video though another op amp, the contrast could be controlled by varying the gate of the op amp. Similarly, the horizontal and vertical sync pulses could be controlled in amplitude by another op amp which would set brightness. These signals could then be added back together to form composite video to send on to the monitor. Figure 3 is a block diagram of this approach.

However, in searching the commercial linear circuits a device called a liminance processor (a RCA CA 3144G) was discovered. This device claimed to control brightness and contrast in response to voltage at the appropriate pins. One of these devices was obtained from a local parts house and bench tested to verify its claims. The circuit was

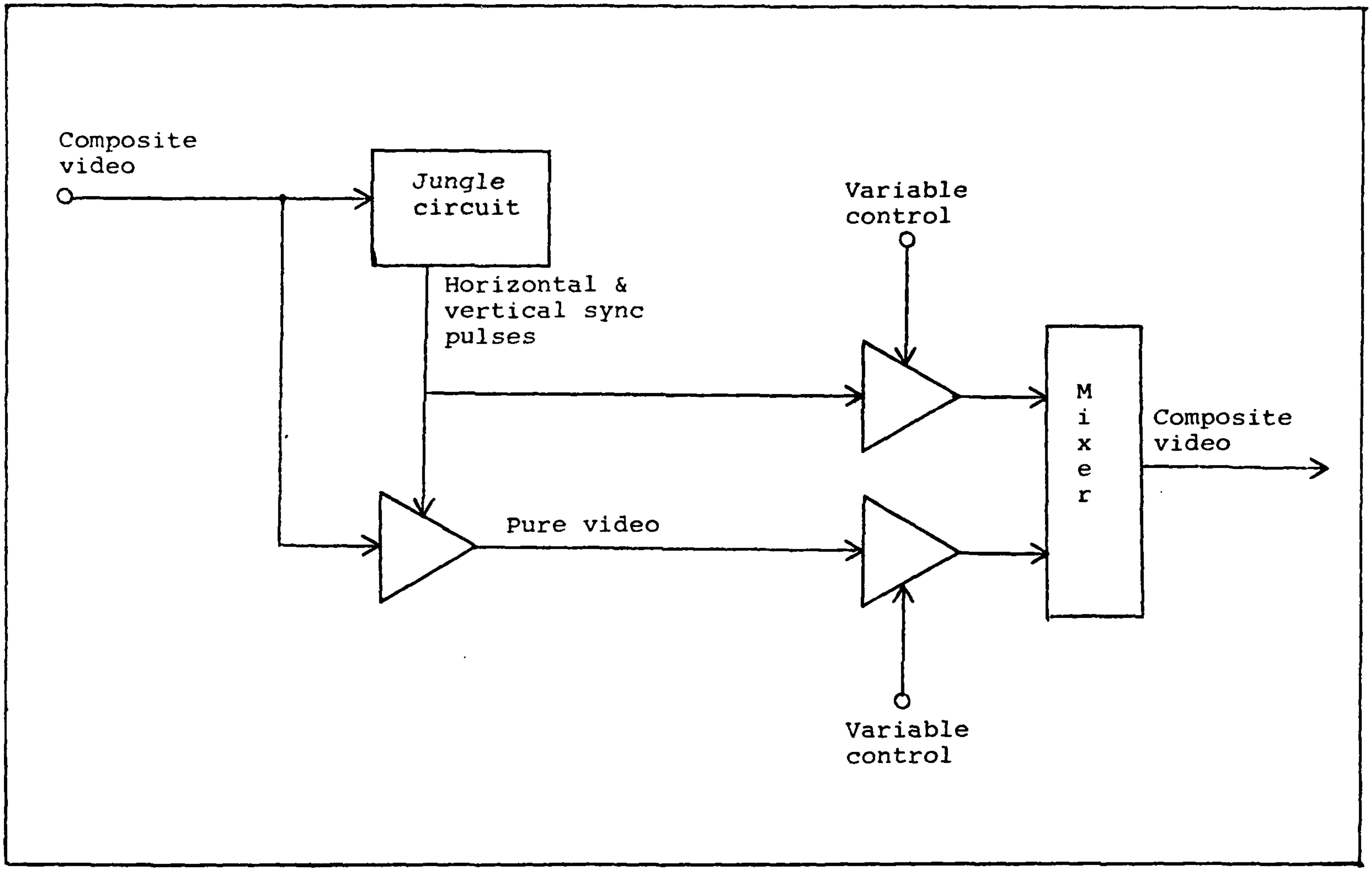



Fig. 3  Video Processing Diagram

found to control contrast over a one volt peak-to-peak signal and brightness over a four volt range. The output of the circuit is inverted, so the signal needs to be inverted again before it is passed on to the monitor. Figure 4 shows the wiring of the circuit.

In verifying the output of the liminance processor on a monitor, it was noted that although there was adequate contrast control, hardly any control was noticed over brightness. The lack of brightness control is caused by the method of DC restoration. The RCA monitor's DC restorer does not provide extensive control over the brightness range in the video signal. The monitor circuitry compensates for this limited range via adjustments in the manual brightness circuit.

At this point it becomes apparent that direct modification of the monitor will be necessary. Either all the capacitive coupling will have to be removed or the voltage of the DC restorer directly controlled. The latter appears the easier and is reversible. A simple toggle switch could restore the monitor to brightness control via its front panel knob.

One method of controlling brightness could be in the use of a transistor to replace the manual brightness control. A transistor (SK 3024) was selected that could provide the appropriate voltage swings (35-90 volts) for full brightness control. This control is obtained by regulating the base voltage of the transistor with a digital-

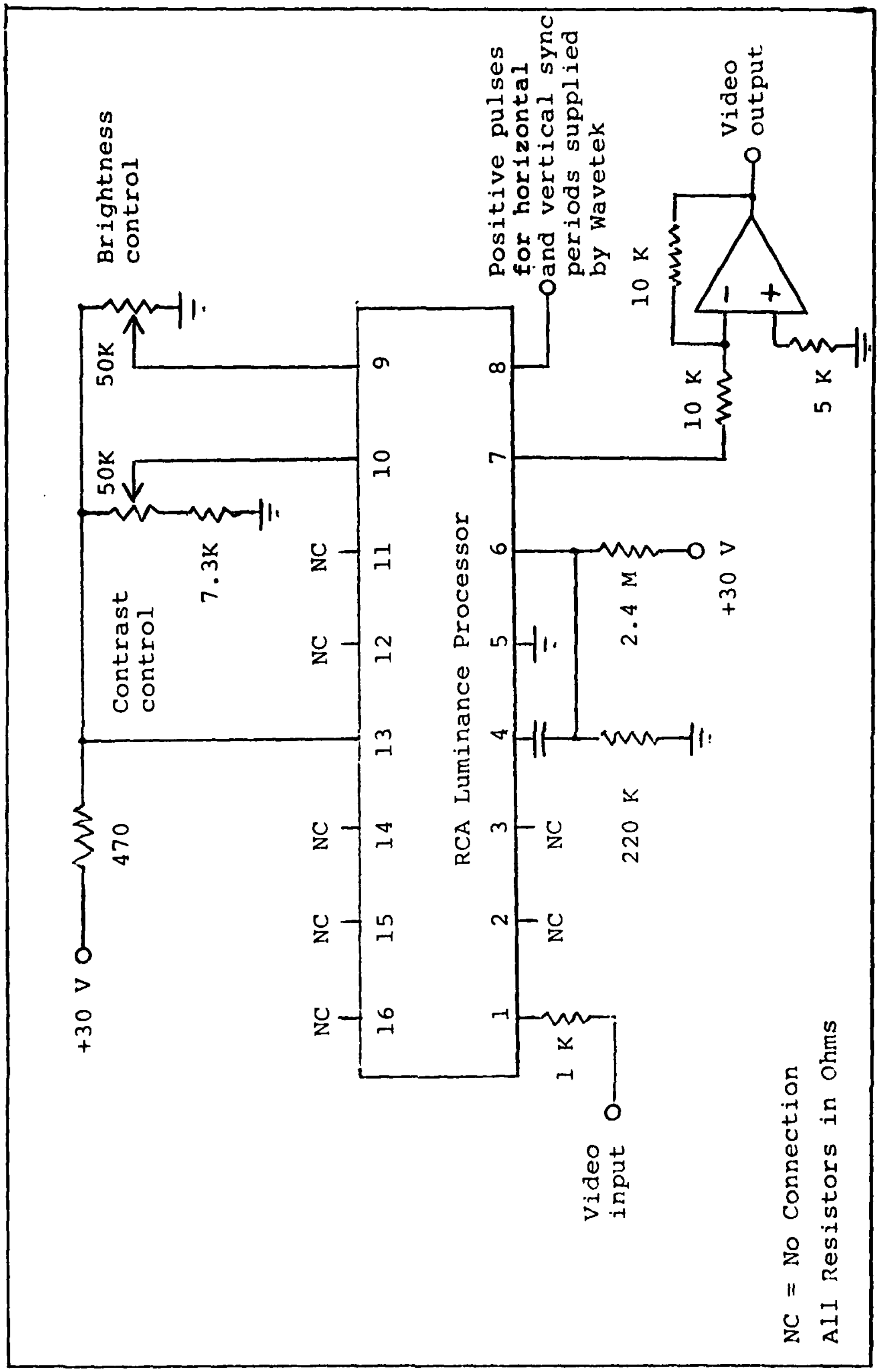



Fig. 4 Wiring Diagram for Luminance Processor

to-analog converter (DAC).

Detection

Once the video processing section was roughly outlined, thoughts turned to verifying that the levels requested were indeed those levels produced. Two ideas were considered: one uses a "light pen" (that is, a photo diode) manually drawn across the face of the monitor, the other uses a stationery array of photo diodes.

In the first scheme, the light pen measures the peaks and valleys of the sine wave gratings as it passes across the face of the screen. However, a potential problem exists in the velocity of the pen's travel. As the frequency of the sine wave grating increases more grating bars are present on the screen. If the pen is moved too quickly, some of the peaks or valleys may be skipped. Training an operator on the proper speed of pen travel may be possible, but not necessary if the motion can be eliminated.

The second proposal eliminates any motion errors since the array is stationery. The array could be positioned across several grating bars allowing each diode to measure the luminance within its field of view.

To determine the size of the photo diode necessary, the resolution of the monitor needs to be determined. The monitor is capable of producing 240 lines. The width of the CRT is 7 inches. That gives 240 / 7 = 34 lines per inch. To preclude the diodes of the array from aligning on the borders of every line pair and thus showing no variance in the signal, at least twice the number of diodes would be needed or 68 diodes per inch. This gives a diode opening of .015 inches (.334 mm).

A search of current optoelectronic catalogs revealed that the smallest photo diodes available had a photo sensitive area of .039 inches (Ref 6,7). While this is only slightly larger than required, the TO-18 packaging is .25 inches wide. This allows only 4 diodes per inch when placed in a linear array, a factor of 17 off from the desired 68 diodes per inch. The possibility of constructing an array to achieve the necessary resolution form individual diodes appears to be impossible.

However, a prefabricated linear array was located that exceeds the above specifications. The 1024-G linear array made by Reticon is a 1 inch array with 1024 diodes packed in that inch. The aperture of each diode is .015 mm which is 25 times finer than necessary. Since this is in excess of the monitors' resolution, the Reticon array was chosen over any self-constructed array. Additionally, Reticon makes a sample-and-hold amplifier for use with their arrays. The availability of a prewired, integrated array and amplifier should speed overall construction of the project.

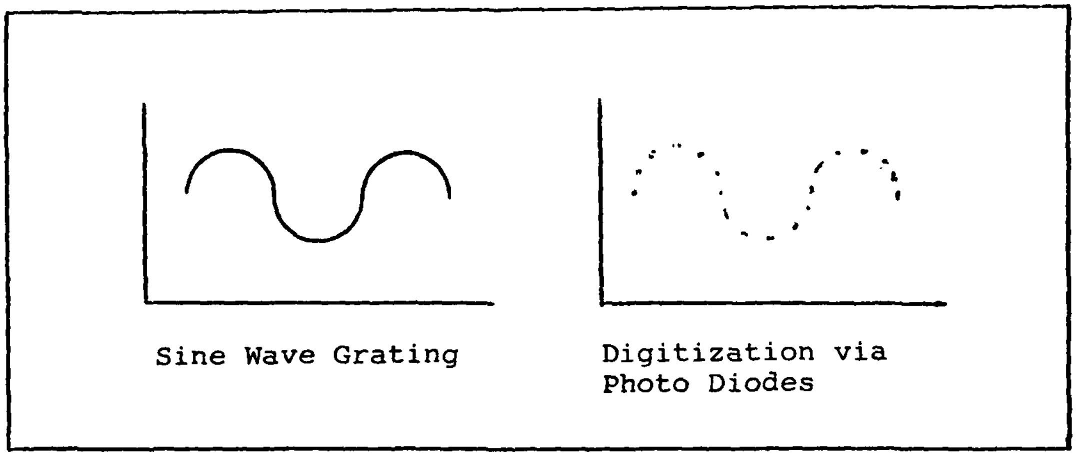



Fig. 5 Sine Wave Approximation

## Calculation and Correction

Now that a means of detecting the luminance of the monitor has been proposed, a method of calculation and correction of the luminance needs to be found. In particular, the device needs a way to determine what the produced luminance values are, compare those values to the desired values, and provide corrections to the video circuitry. The solution lies in the use of a microcomputer.

A microcomputer, through the use at an analog-to-digital converter (ADC), could read the values of individual diodes in the array. It would be approximating the monitor's sine wave grating in a fashion shown in Figure 5. With the sine wave digitized, a simple sorting could find the highs and lows of the signal. By averaging the highs, $L_{max}$ can be determined. $L_{min}$ is similarly found by averaging the lows. From $L_{max}$ and $L_{min}$, $L_{avg}$ can be established. Comparison can then be made between desired

$L_{avg}$ (brightness) and calculated $L_{avg}$. The difference between the two could be used to change a DAC controlling the brightness transistor. Appendix A details the relationship between base voltage and collector voltage. It also shows the relationship between the collector voltage (brightness setting) and foot-Lamberts produced on the CRT.

Using Equation 2, contrast can be calculated. By directly controlling the contrast voltage pin of the luminance processor with another DAC, control of the $\Delta$ portion of the equation can be obtained. Taking into consideration any changes made to brightness, appropriate changes can be made to the $\Delta$ portion to achieve the desired contrast.

Figure 6 is a block diagram of the major functional parts of the design.

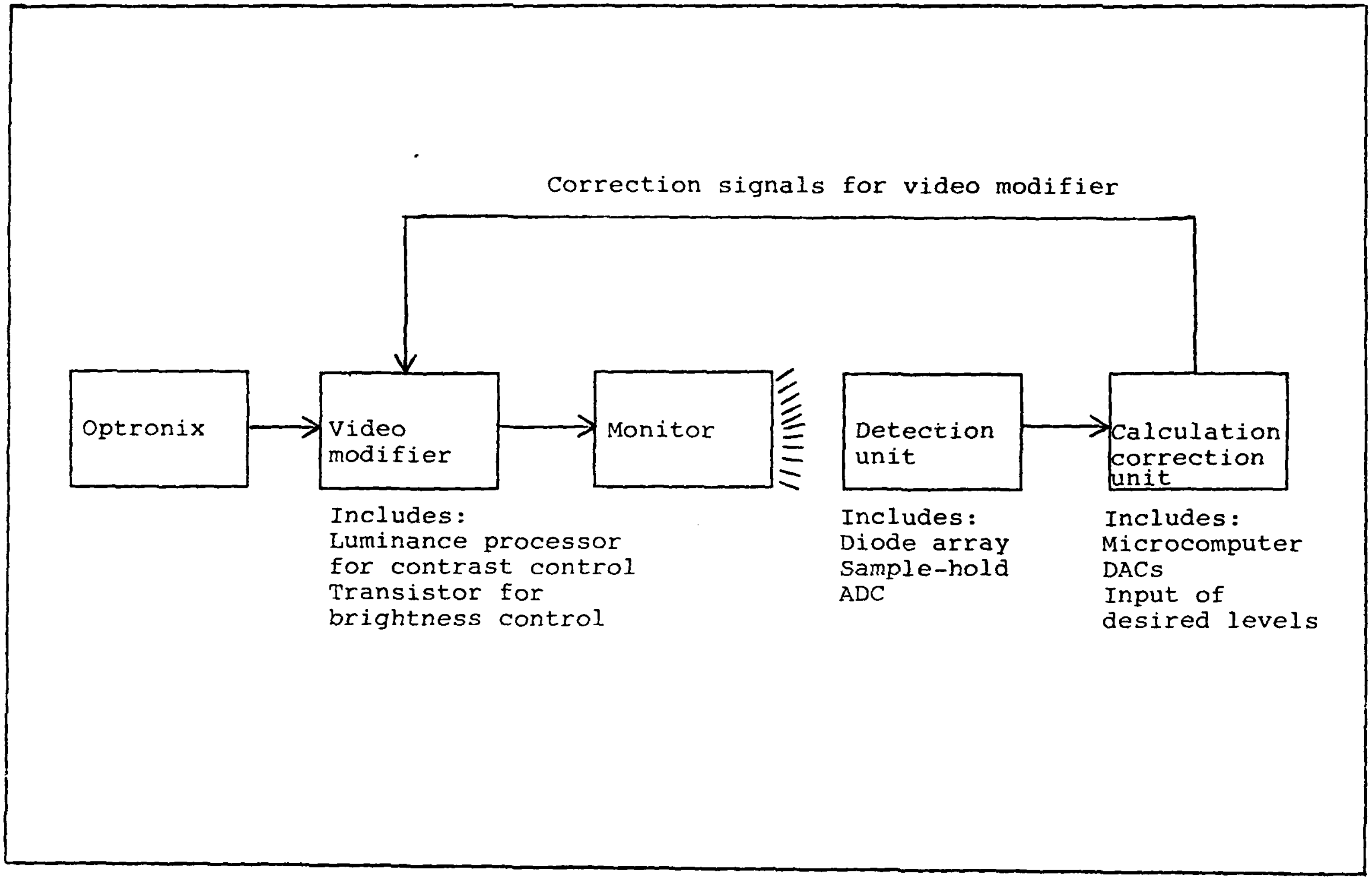



Fig. 6 Functional Block Diagram of Design

## III Component Selection

System requirements are now defined in order to aid in selection of ADCs, DACs, and the computing element.

### Requirements

At present there is no definitive source on the absolute accuracies needed in stimuli generation. The following accuracies are based on the desires of AMRL.

The average luminance or brightness should be controlled to within .2 foot-Lamberts (fL) of the desired level. The range of brightness AMRL would like to work in is 2 - 40 fL. The number of brightness levels is then 38 /.2 = 190. An 8 bit DAC provides 256 states and can adequately cover the needed range of brightness control.

The range of contrast desired is 1.00 to .01. Therefore, there exist 100 levels of contrast for any brightness level. At the low end of the monitor's brightness range, the increments necessary for .01 contrast at 2 fl equal .02 fL. The range of brightness from 2 - 40 fL implies the photo diode array should detect 38 /.02 = 1900 levels of luminance. An 11 bit ADC would provide 2048 levels to interpret the Reticon array. The same argument holds for the DAC that controls the contrast voltage levels of the luminance processor.

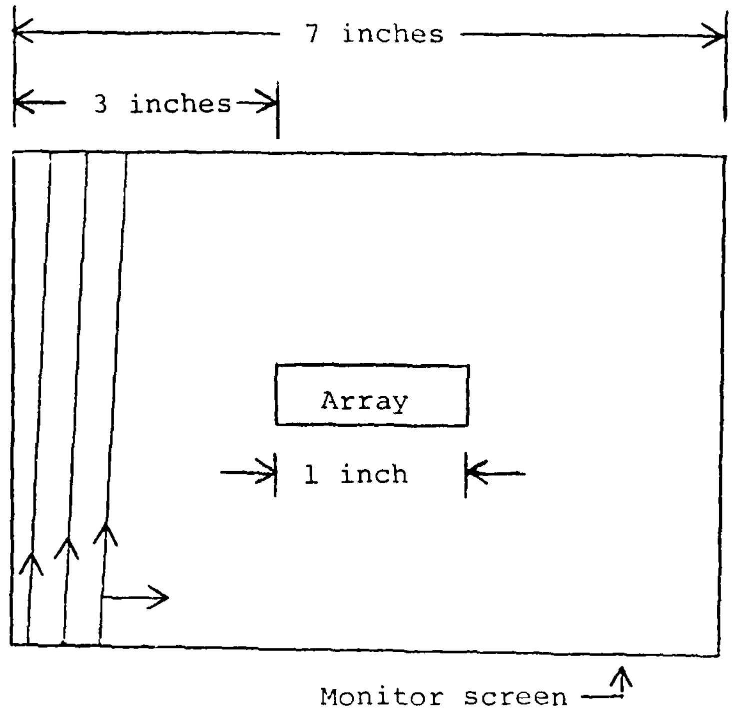
## Converters

The selection criteria of the DACs do not impose any severe limitations. The DACs will not be operating in a hostile environment, so temperature ranges are not extreme. DACs designed for operation in the $0^{o} - 70^{o}C$ range are quite adequate. The speed of conversion does not have to be extremely fast nor does the input have to conform to any particular format (BCD, twos-complement, etc) since the microcomputer can format the input before transmission. Essentially, the only criteria left is cost. In each case of DAC selection the least expensive was found. The 8 bit DAC selected for brightness control was a Datel UP8BC. Since 11 bit DACs are not commonly available, the 12 bit Datel HZ12BGC was chosen for contrast control.

The selection of the ADC, though, must consider speed of operation. The scanning of the photo diode array must start from some reference signal. This insures that repetitive readings of the diodes will be consistent, and that each diode will be exposed to the sine wave grating for the same amount of time.

The present plan is to measure luminance in the middle of the screen. If the vertical sync pulse is used to start the array measurements, then the last diode of the array must be sampled before the electron beam (E-beam) of the CRT scans over that diode again. This one would insure that all the diodes will have been exposed to the same stimulus, one pass of the E-beam, for the same length of time. The RCA monitor is non-interlaced and refreshes the CRT once every 19 msec. An oddity of this monitor is that it scans horizontally. Its vertical sync signal comes as the E-beam reaches the right side of the CRT. Therefore, the rate at which the E-beam travels across the face of the screen is 7 inches / 19 msec = .37 inches/msec. Since the array will be held near the center of the screen, the distance from the left edge of the CRT to the left edge of the array is about 3 inches. Intuitively one could reason that if the last array diode is sampled before the E-beam has traveled 3 inches from the left edge of the CRT, adequate spacing would be insured. The time for 3 inches of travel of the E-beam is 8.1 msec. This should correspond to the total time of sampling the array. Each diode in the array would be sampled in 8 usec to have all 1000 diodes sampled in 8 msec. Figure 7 shows the relationship.

Approximating aperture and uncertainty delays of the Reticon sample-and-hold circuitry to less than 1 usec (Ref 8) would leave a hold time of 7 usec for each diode. A 12 bit ADC that converts in 7 usec costs approximately $250.00 (Ref 9). However, if another sample-and-hold circuit is introduced between the Reticon sample-and-hold and the ADC, it could retain the value of interest while the array continues to scan. Since the array exceeds the required resolution, every diode need not be sampled. In fact, the second sample-and-hold only needs to acquire every fifteenth diode to achieve the required resolution. The




E-beam traces each line from bottom to top and traces the entire screen from left to right. The E-beam travels 1 inch of horizontal distance in 2.7 msec.

Fig. 7 Diode Array Position and E-beam Trace Relationship

SHM-IC-1 sample-and-hold made by Datel has an acquisition time of 5 usec and would work adequately. With the use of this second sample-and-hold, the conversion time of the ADC needs to be less than 120 usec which is the time interval between every fifteenth diode. Datel's HX12BGC ADC meets this speed and is the least costly of all 12 bit ADCs operating the usec range. The combined cost of the SHM-IC-1 and the HX12BGC is only $104.00, less than half of an ADC that could operate at 7 usec without the extra sample-and-hold.

Computer

In addition to the requirements stated earlier, the selection of a computer must also consider input-output (I/O) capabilities, memory capacity, instruction speed, physical size, and cost.

The input requirements for this system consist of 12 bits from the ADC, 8 bits for the desired brightness input (2 BCD digits ranging from 2 to 40), and 8 bits for the desired contrast input (2 BCD digits ranging from 0 to 99). Thus a total of 28 input lines are required. For output, the computer needs to control a 12 bit DAC for contrast level and an 8 bit DAC for brightness level. Additionally there should also be a bit to turn on and off a light to indicate to the operator when the system is within tolerance. Thus a total of 21 bits are needed for output.

Memory requirements are divided into random access memory (RAM) and electrically programmable read only memory (EPROM) needs. The RAM should be large enough to hold the values of all the diodes sampled. These values are 12 bits wide which will require 2 bytes to store. There are 69 diode values to store requiring 138 bytes. Also needed is 1 byte to hold the desired contrast level, 1 byte to hold the desired brightness level, 1 byte to hold the value for the brightness DAC, and 2 bytes to hold the value for the contrast DAC. A scratch pad area of 50 bytes will probably be needed for program calculations and manipulations. This gives an approximate need of 195 bytes of RAM. The EPROM will hold the main program and look-up tables for the DACs. The estimated size of the main program is 1000 (1K) bytes. The contrast look-up table has 1900, 2 byte values or 3.8K bytes total. The brightness table needs 190 bytes. Therefore, the EPROM requirement is 5K bytes.

The only critical requirement for speed is to insure that the ADC gets read before the next diode of interest is sampled. The time between samplings is 120 usec. Any microprocessor operating at 1 MHz can easily handle this requirement.

The computer selected was a Mostek MDX. This is a Z-80 based system that consists of user configurable modules. The memory can be arranged in 2K increments of any combination of RAM and EPROM up to a limit of 12K. This versatility will allow the program to be verified in RAM where changes can be made before placing the program in EPROM.

There are a total of 256 eight bit ports available for I/O. This is more than adequate for system needs.

The average instruction speed is 6 usec. This allows more than enough time to store the value of the ADC between diode samplings. Also the instruction set contains 16 bit load and arithmetic instructions. These instructions will be of great help in handling the 12 bit data of the ADC.

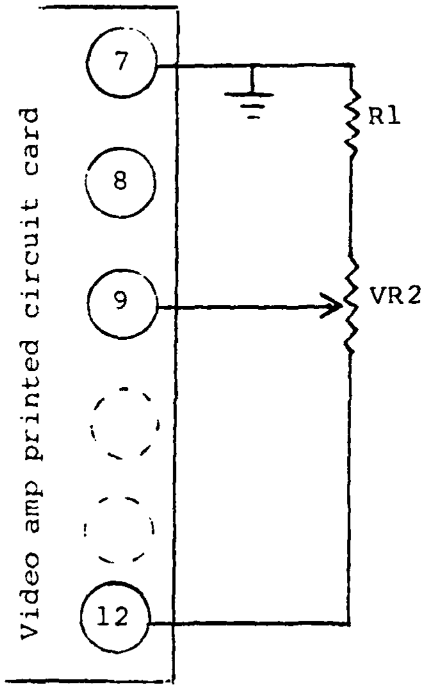
Another advantage of the Mostek computer is its size. It is one of the smallest systems available, hence it will be more portable and take up less room.

# IV Construction

## Video Modifier

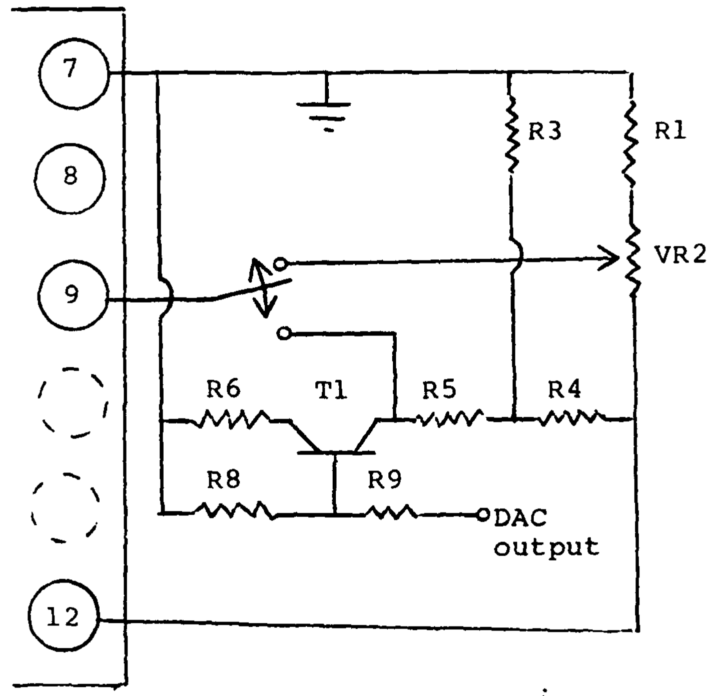
As explained in Section II, brightness control is provided by a SK 3024 transistor. Transistor wiring and implementation into the present brightness control circuit is shown in Figure 8. The brightness DAC's output is applied to a voltage divider on the base of the transistor. It is not necessary for the collector voltage to swing from 35 to 90 volts. Figure 9 shows that voltage range of 33 to 60 volts will provide 2 to 40 fL of screen luminance. Another voltage divider brings the supply voltage to 61 volts and the base voltage keeps the collector voltage in the 33 to 60 volt range. Table 1 gives the screen luminance in terms of input code to the DAC.

The circuit controlling contrast has a minor problem. The bench tested circuit of Figure 4 worked well when blanking pulses were provided by a Wavetek waveform generator. However, when blanking pulses were supplied by an op amp configured as a comparator (Fig. 10) the output waveform had a noticeably wider blanking pulse. The effect of this wider pulse could be seen on the bottom edge of the monitor as a ragged line. Additionally, the contrast control of the luminance processor is now erratic and unpredictable. At present no solution or explanation for the problem has been found.




a) Present Wiring

R1 = 47K
VR2 = 100K
R3 = 47K
R4 = 18K
R5 = 120K
R6 = 10K
R7 = 270
R8 = 100
T1 = SK 3024




b) Modification of Wiring Allowing Digital or Front Panel Control

Fig. 8 Modification of Monitor Brightness Circuit

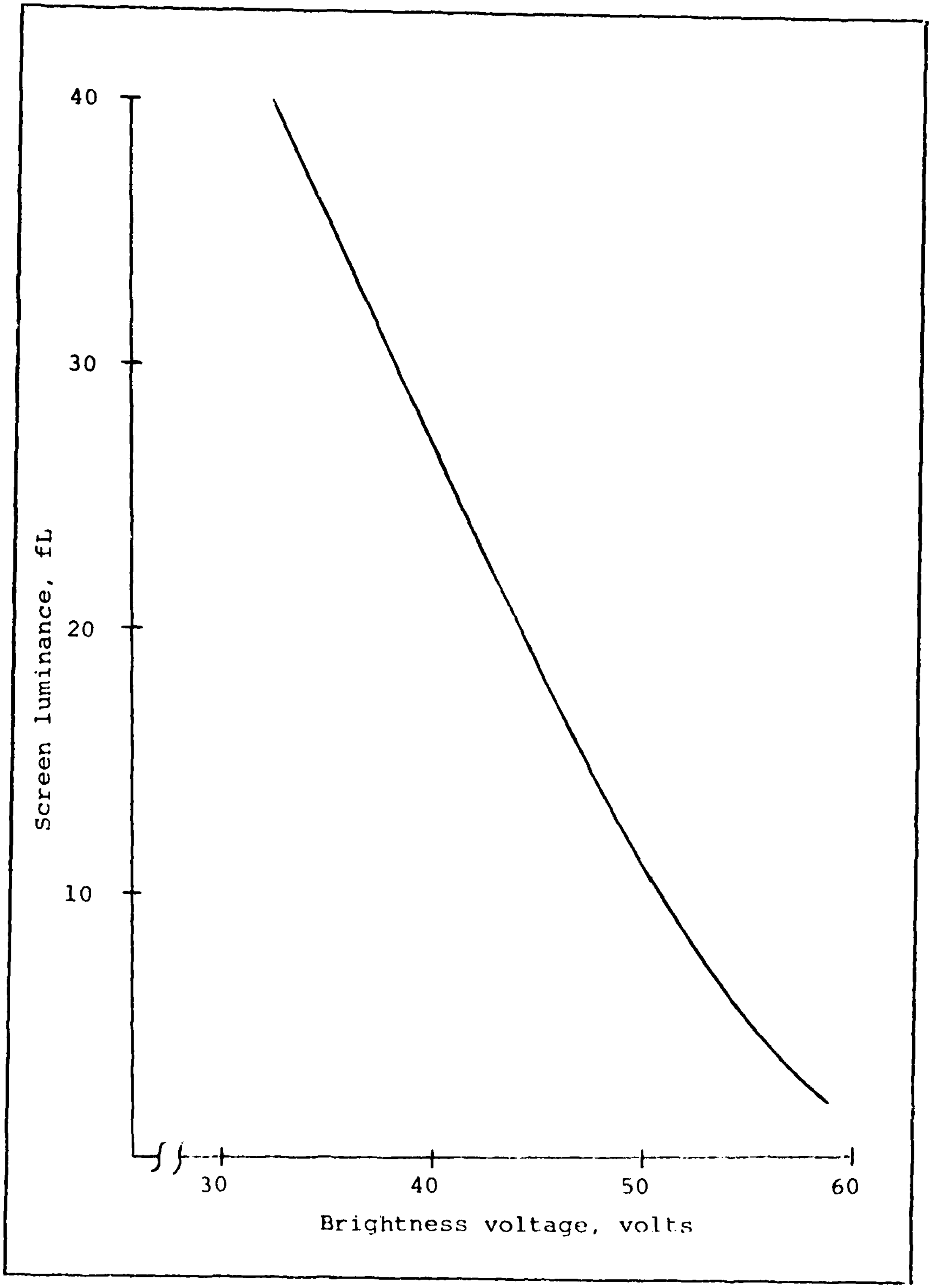



Fig. 9 Brightness Voltage vs Screen Luminance

TABLE I

Output Code for Desired Luminance

| Luminance (fL) | DAC Code (decimal) | Luminance (fL) | DAC Code (decimal) |
|---|---|---|---|
| 2 | 64 | 21 | 174 |
| 3 | 72 | 22 | 178 |
| 4 | 80 | 23 | 182 |
| 5 | 87 | 24 | 187 |
| 6 | 94 | 25 | 191 |
| 7 | 100 | 26 | 195 |
| 8 | 107 | 27 | 200 |
| 9 | 113 | 28 | 204 |
| 10 | 119 | 29 | 208 |
| 11 | 125 | 30 | 212 |
| 12 | 130 | 31 | 216 |
| 13 | 136 | 32 | 221 |
| 14 | 141 | 33 | 225 |
| 15 | 146 | 34 | 230 |
| 16 | 151 | 35 | 234 |
| 17 | 156 | 36 | 239 |
| 18 | 160 | 37 | 244 |
| 19 | 165 | 38 | 249 |
| 20 | 170 | 39 | 254 |

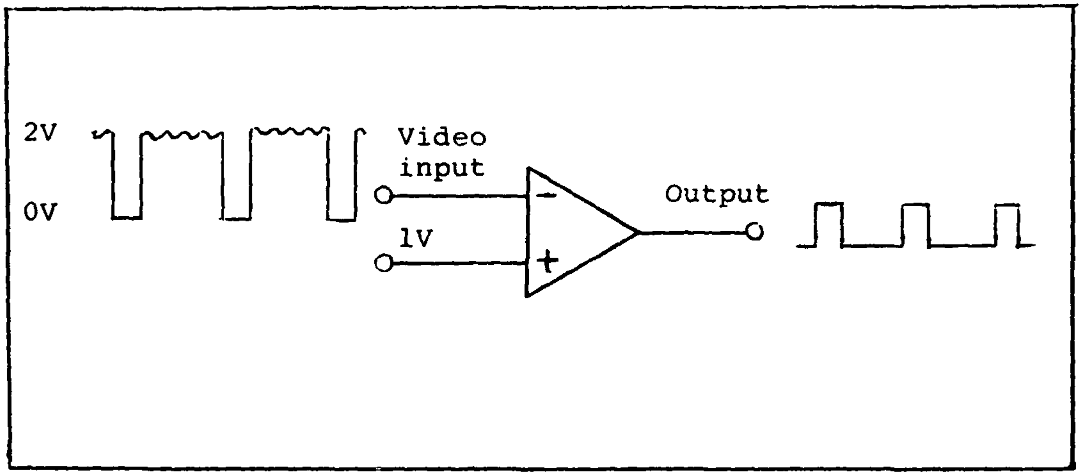



Fig. 10 Creation of Positive Blanking Pulses

Video Detection

An important element of the Reticon array is its timing Too much exposure will cause saturation, and an unusable output. Figure 11 graphs the output charge versus the exposure of the array. Exposure is determined by the scan time of the array. To determine if an 8 msec scan time was adequate to measure up to 40 fL the following calculations were made:

Definition, $1 \text{ fL} = 1.076 \times 10^{-3}$ lumen / $cm^2$

definition, $1 \text{ lumen} = 1.538 \times 10^{-3}$ Joule / sec

then, $1 \text{ fL} = 1.655 \times 10^{-6}$ Joule / sec . $cm^2$.

$$\text{For 8 msec, } 1 \text{ fL} = (1.655 \times 10^{-6} \text{ Joule / sec . cm}^2)(8 \text{ msec})$$

$$= 0.0132 \times 10^{-6} \text{ Joule / cm}^2$$

$$40 \text{ fL} = 0.5296 \times 10^{-6} \text{ Joule / cm}^2.$$

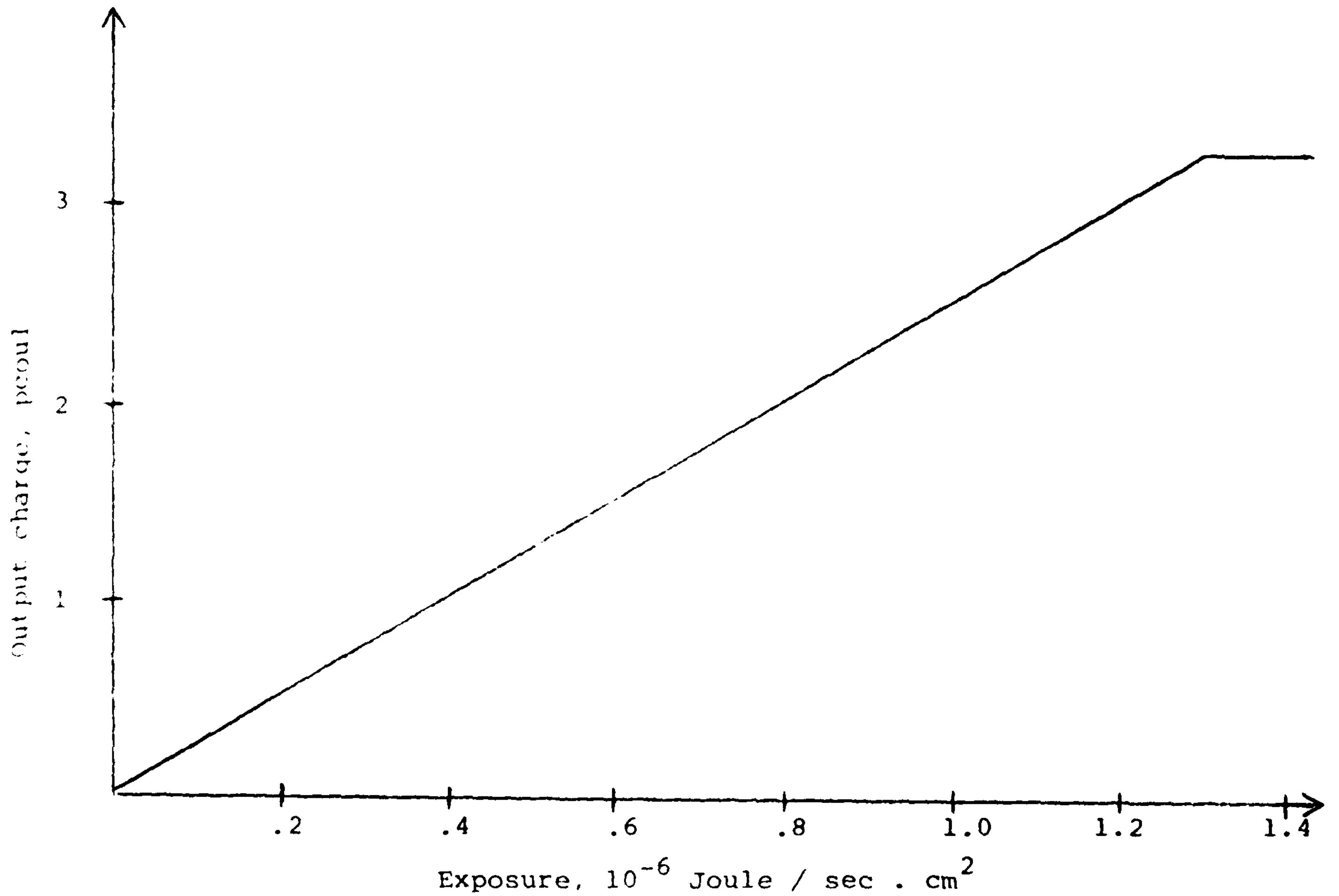



Fig. 11 Exposure vs Output Charge

Thus 40 fL of luminance can be detected by the array without saturation in an 8 msec scan time. This scan time equates to a clock frequency of 125 KHz in order to sample the 1,000 element array in 8 msec.

The vertical sync, which can be detected from the circuit of Figure 10, in conjunction with a command from the microprocessor (uP) can start the array and the clock. A simple modulo-15 counter, constructed of 15 flip flops wired in series, provide the timing for selection of diodes to be sampled. The 14th flip flop controls the SHM-IC-1 sample-and-hold. The 15th flip flop triggers the 12 bit ADC, and resets the modulo-15 counter. After the ADC is finished, an interrupt signal is sent to the uP. The uP then stores the data and waits for another value. This process repeats until the array indicates end of scan. Figure 12 shows the relationship between these various components.

## Computer

The computer performs six basic functions. First, it provides a first-guess approximation to the desired contrast and brightness settings. Second, it controls and reads the diode array. Next, it sorts the diode values for $L_{max}$ and $L_{min}$, and produces a calculated $L_{avg}$. Finally, it compares desired with calculated levels to determine if a correction is needed.

Because of the late arrival of the computer no coding

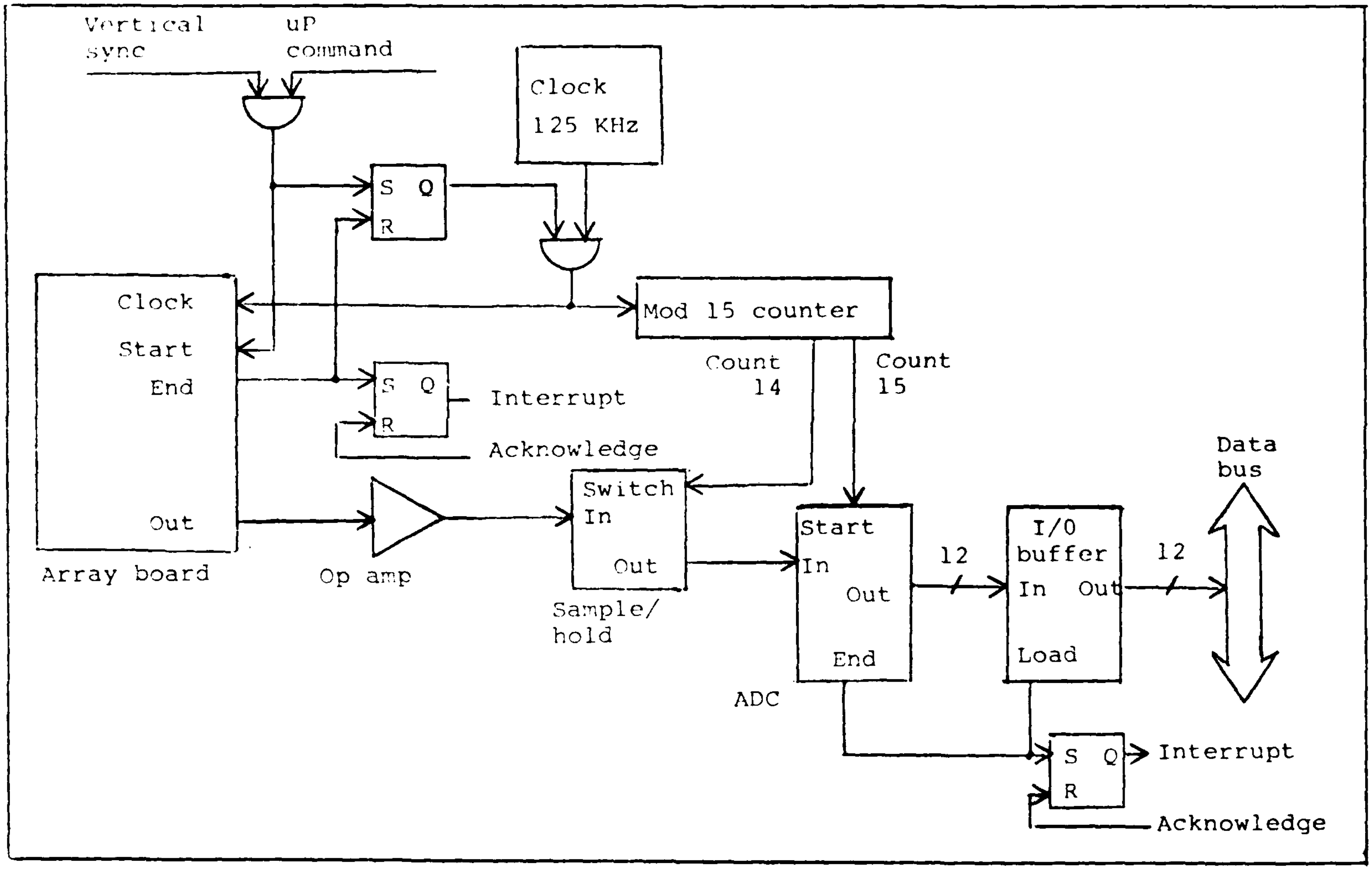



Fig. 12 Block Diagram of Array and ADC Interconnection

has been done. However, flow charts for program operation are contained in Appendix B.

## V Conclusions and Recommendations

### Conclusions

The hardware design and component selection phases of this project are complete. Brightness control is provided over the range of 2 to 39 fL. The contrast control circuit demonstrated adequate ability to regulate the amplitude of sine wave gratings when bench tested. This device will be an important aid in helping scientists further define the capabilities of the human visual system.

### Recommendations

While the contrast circuit worked well when bench tested, it now behaves erratically. The suspected cause of this erratic behavior is the comparator producing the blanking pulses. Once this problem is corrected, the circuit should behave normally and hard wiring can begin.

Hard wiring also needs to be performed on the various data converters and their interface with the uP. The uP programs need to be coded and subsequently debugged. Additionally one more look-up table needs to be calculated for the contrast settings. Enough work remains for a thesis on digital interfacing and software design.

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## Appendix A

### Luminance Data

This appendix describes the relationship between brightness voltage and screen luminance for the CRT that will be used in the proposed system. The luminance of the cathode ray tube (CRT) was measured at varying voltage levels of the brightness circuit. Luminance was measured with a Spectra model Pritchard photometer. While the center of the screen is the area where the diode array will operate, readings were taken at eight additional locations on the CRT. Figure 13 shows these locations. Voltage was measured by a 4 1/2 digit Fluke multimeter at pin 9 of the video amp card inside the CRT. Table II presents the luminance data for the nine locations.

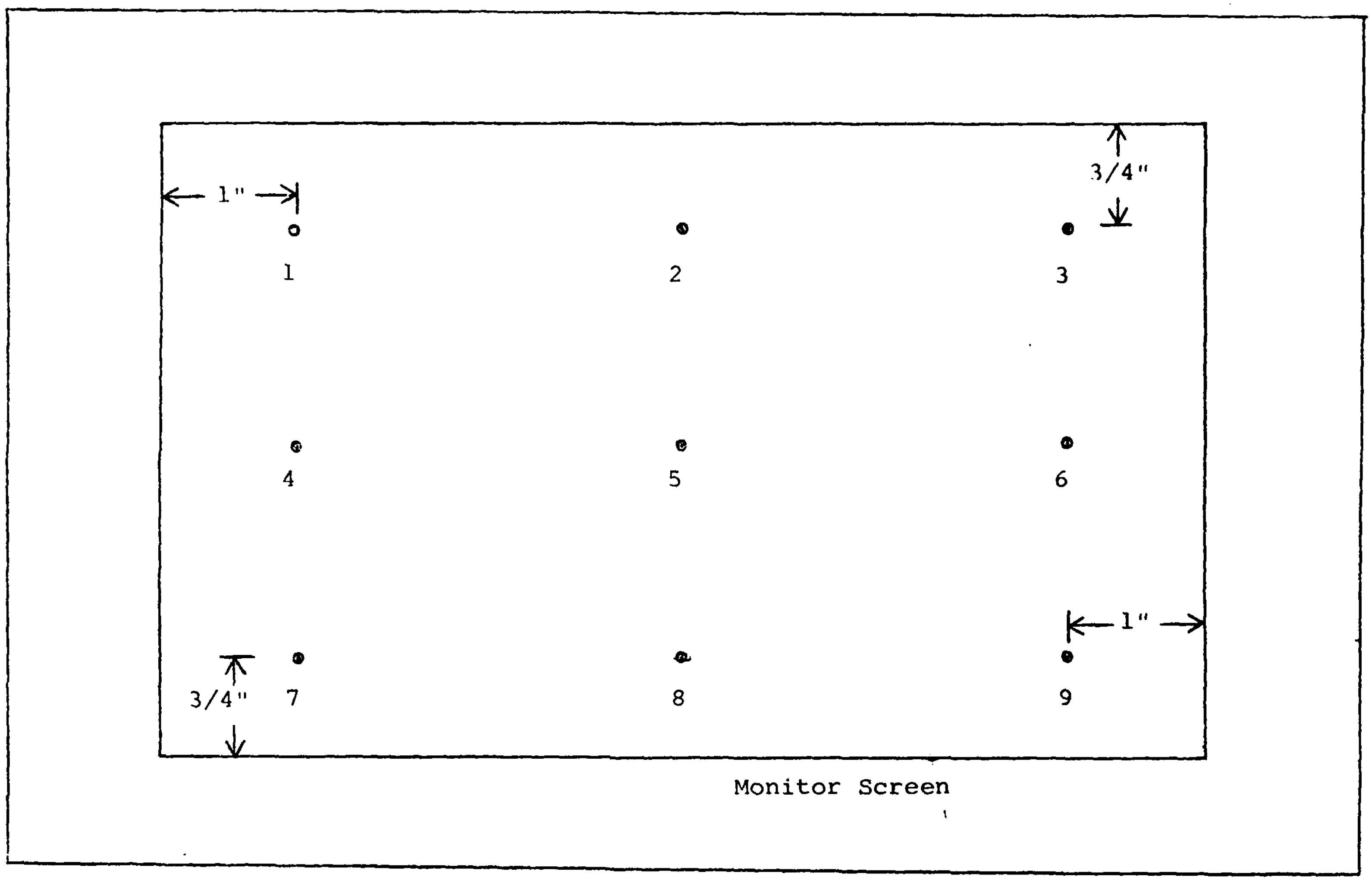


Fig. 13 Location of Luminance Readings

Table II

Luminance Data

| Voltage | Luminance in fL by location | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| V | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 33.6 | 33.6 | 36.1 | 38.9 | 32.3 | 38.5 | 37.4 | 37.0 | 35.5 | 34.7 |
| 38.1 | 27.3 | 30.1 | 31.9 | 26.4 | 30.8 | 30.5 | 30.0 | 29.2 | 28.4 |
| 43.0 | 20.5 | 22.3 | 23.7 | 19.4 | 22.6 | 22.5 | 22.0 | 22.0 | 21.2 |
| 48.1 | 13.1 | 14.6 | 15.2 | 12.2 | 14.4 | 14.2 | 14.2 | 14.4 | 13.6 |
| 53.1 | 6.7 | 7.6 | 7.9 | 6.2 | 7.2 | 7.2 | 7.6 | 7.5 | 7.0 |
| 63.0 | 1.0 | 1.0 | 1.0 | 0.8 | 0.8 | 0.9 | 0.9 | 0.9 | 0.8 |
| 68.0 | 1.0 | 1.0 | 1.0 | 0.8 | 0.8 | 0.9 | 0.9 | 0.9 | 0.8 |
| 83.0 | 1.0 | 1.0 | 1.0 | 0.8 | 0.8 | 0.9 | 0.9 | 0.9 | 0.8 |

## Appendix B

## Computer Routines

This appendix provides flow charts for the proposed computer program. The program is divided into seven routines: main, initialize, read array, sort, average, brightness correction, and contrast correction.

### Main Program

The main routine is merely an integrator for the calls to the various subroutines. The routine begins by clearing the data locations where the diode values will be stored. Variables and counters are also reset. The sequence of subroutine calls is given in Figure 14. A fixed time delay may be necessary before the call to the read array subroutine is made. This delay is to allow settling of the video modification circuits. The delay could also be used to allow time for positioning of the diode array. The delay could then be terminated via an operator signal.

### Initial Guess Subroutine

This routine begins by reading the inputs for the desired brightness and contrast levels. The program then finds a DAC code that corresponds to the requested level. The code is then sent to the DAC to provide approximate

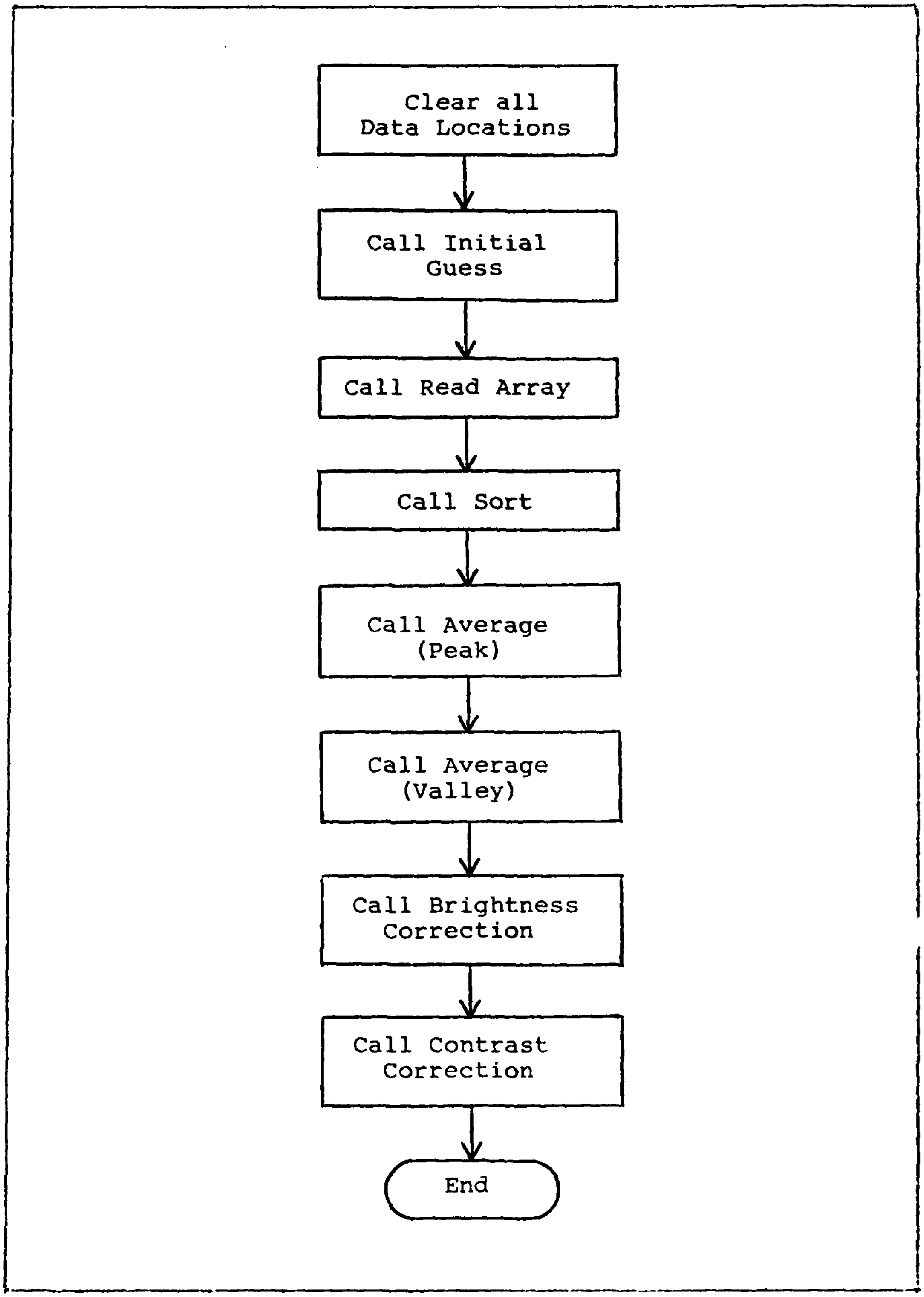


Fig. 14 Main Program Flowchart

brightness and contrast settings for the video signals. A flowchart depicting this subroutine is given in Figure 15.

### Read Array Subroutine

The read array routine (Figure 16) sends the signal that starts the Reticon array and video detection circuitry. After starting the array the program waits until the ADC has a diode value converted and loaded into an I/0 buffer. Since the data is 12 bits wide, two 8 bit ports will be needed to transfer the data. The data is coded by the ADC in complementary binary; therefore before storing the data a complement can be performed to convert the data to binary form. The routine is exited when the array has scanned all the diodes.

### Sort Subroutine

The sorting subroutine saves the high and low values ($L_{max}$ and $L_{min}$) of the stored diode reading. The algorithm works by successive comparison. Each value is compared to the value preceding it. Those values greater than adjacent values are stored as peaks, and those less than adjacent values are stored as valleys. Figures 17 and 18 flowchart this routine.

### Average (X) Subroutine

After the diodes have been sorted into groups of local

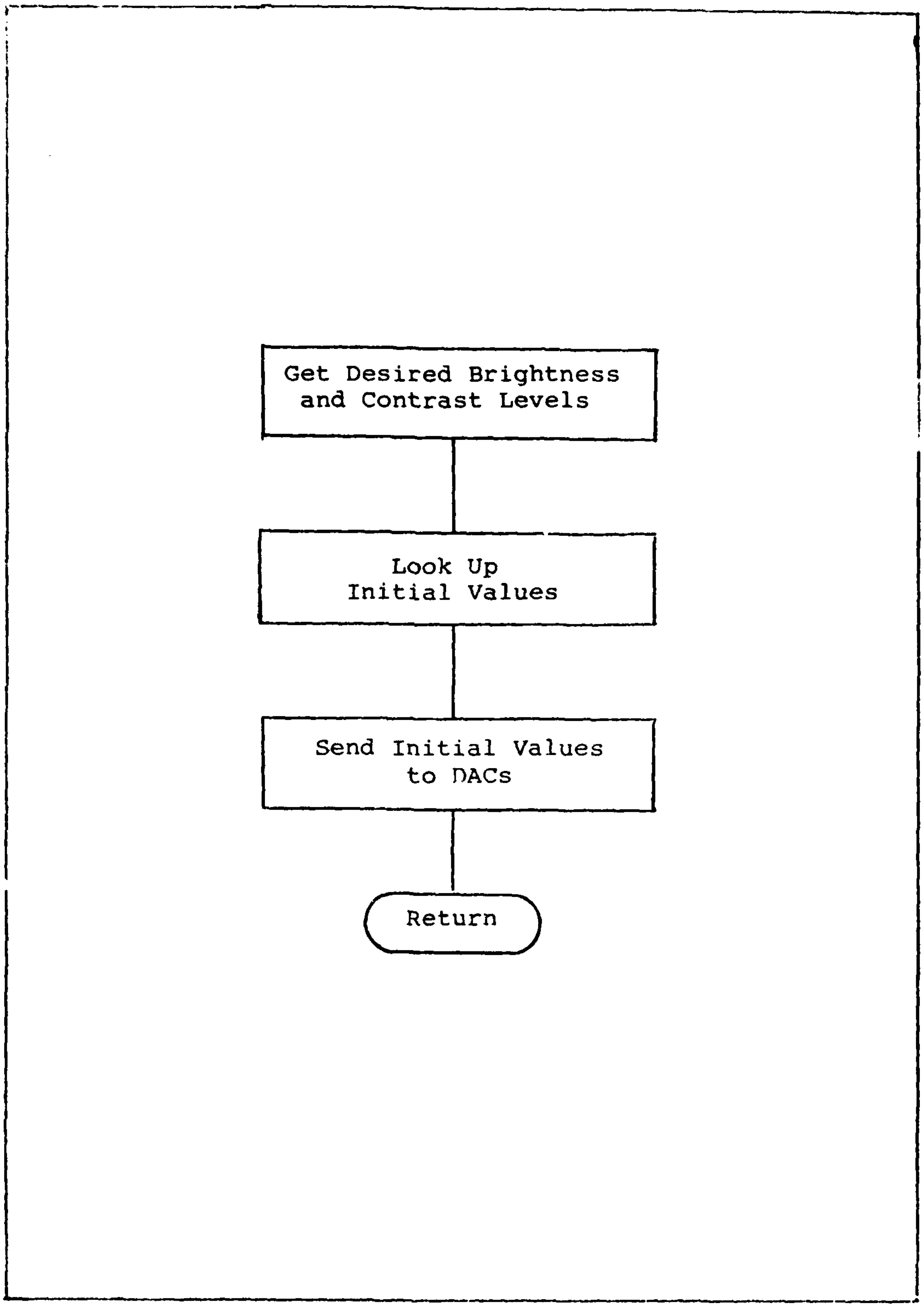


Fig. 15 Initial Guess Subroutine Flowchart

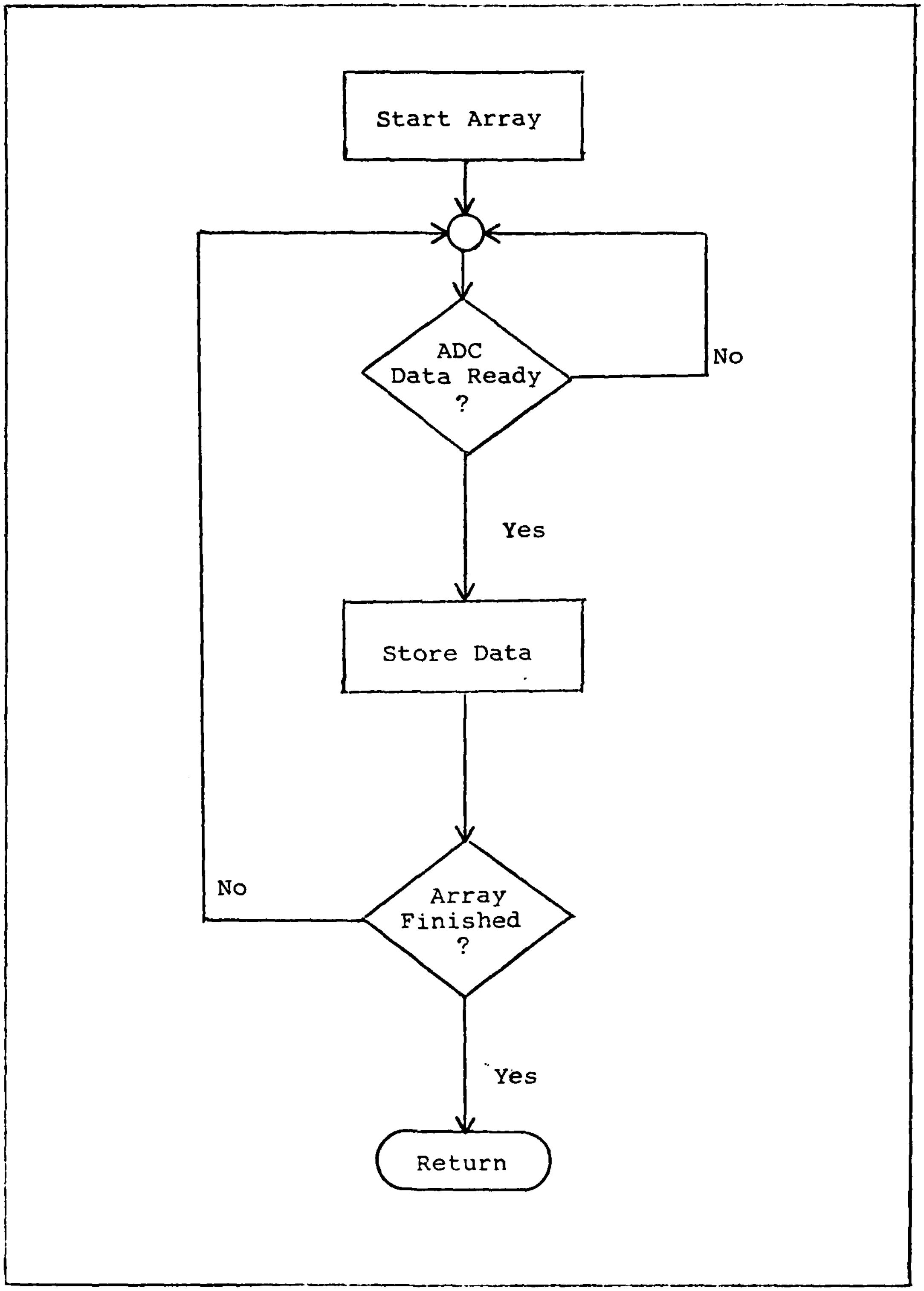


Fig. 16 Read Array Subroutine Flowchart

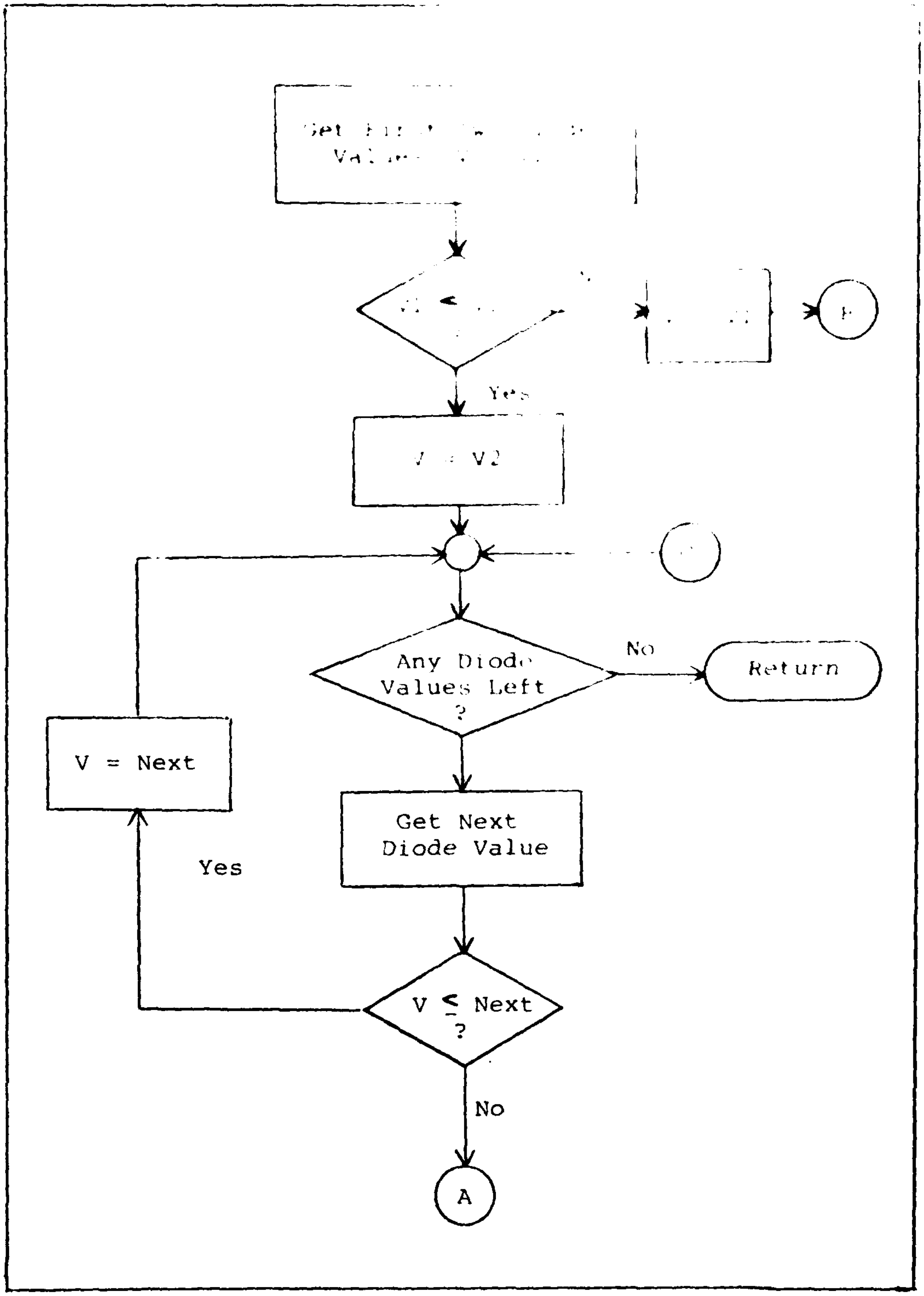


Fig. 17 Sort Subroutine Flowchart (Page 1 of 2)

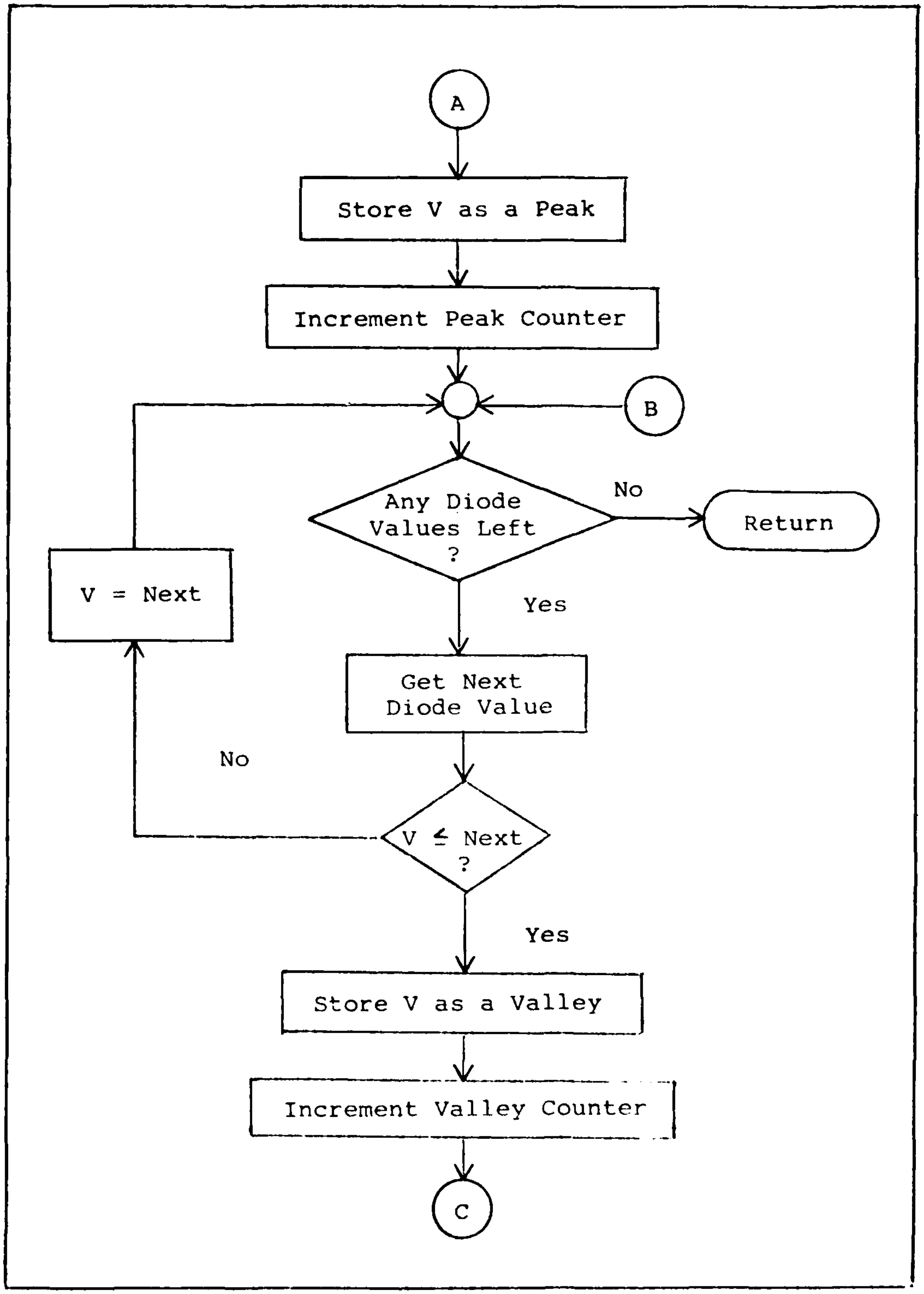


Fig. 18 Sort Subroutine Flowchart (Page 2 of 2)

peaks and valleys, the average subroutine is called. The routine is called twice: once to average the peaks and again to average the valleys. The routine is also passed a parameter (X) for the location of the values to be averaged. The averaging is accomplished by totaling the difference between the first value and each individual value in X (Figure 19). The total of these differences is then divided by the number of elements in X. Finally, the quotient is added or subtracted to the first value of X to obtain the average (Figure 20).

## Brightness Correction Subroutine

With peak average ($L_{max}$) and valley average ($L_{min}$) available, this routine begins by finding the average brightness ($L_{avg}$):

$$L_{avg} = \frac{L_{max} - L_{min}}{2} + L_{min}.$$

The difference between the desired luminance and the calculated luminance provides a correction factor for the brightness setting. The correction factor is applied to the current brightness setting to obtain a new corrected brightness setting. This setting is then sent to the brightness DAC. A flowchart for this routine is given in Figure 21.

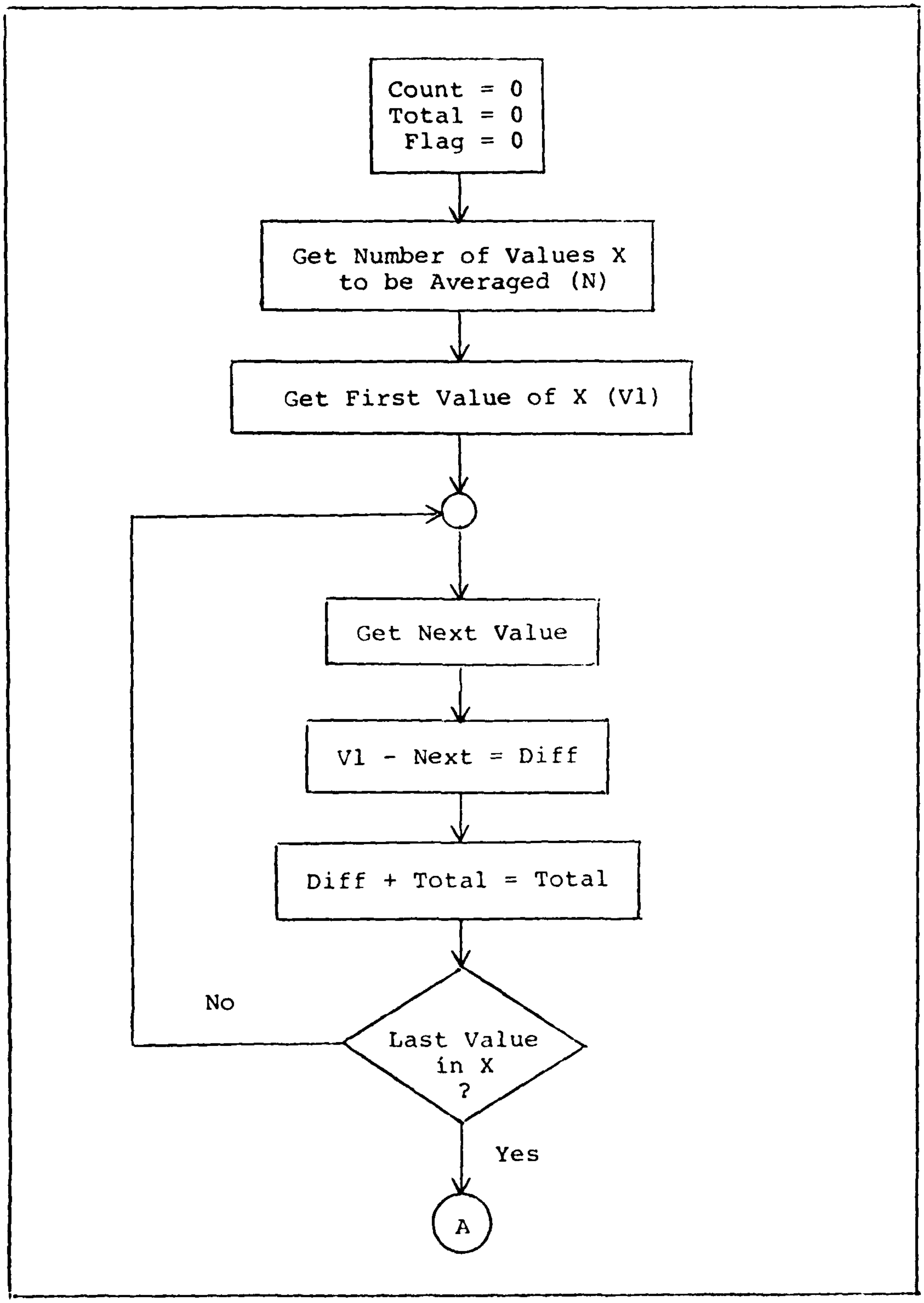


Fig. 19 Average (X) Subroutine Flowchart (Page 1 of 2)

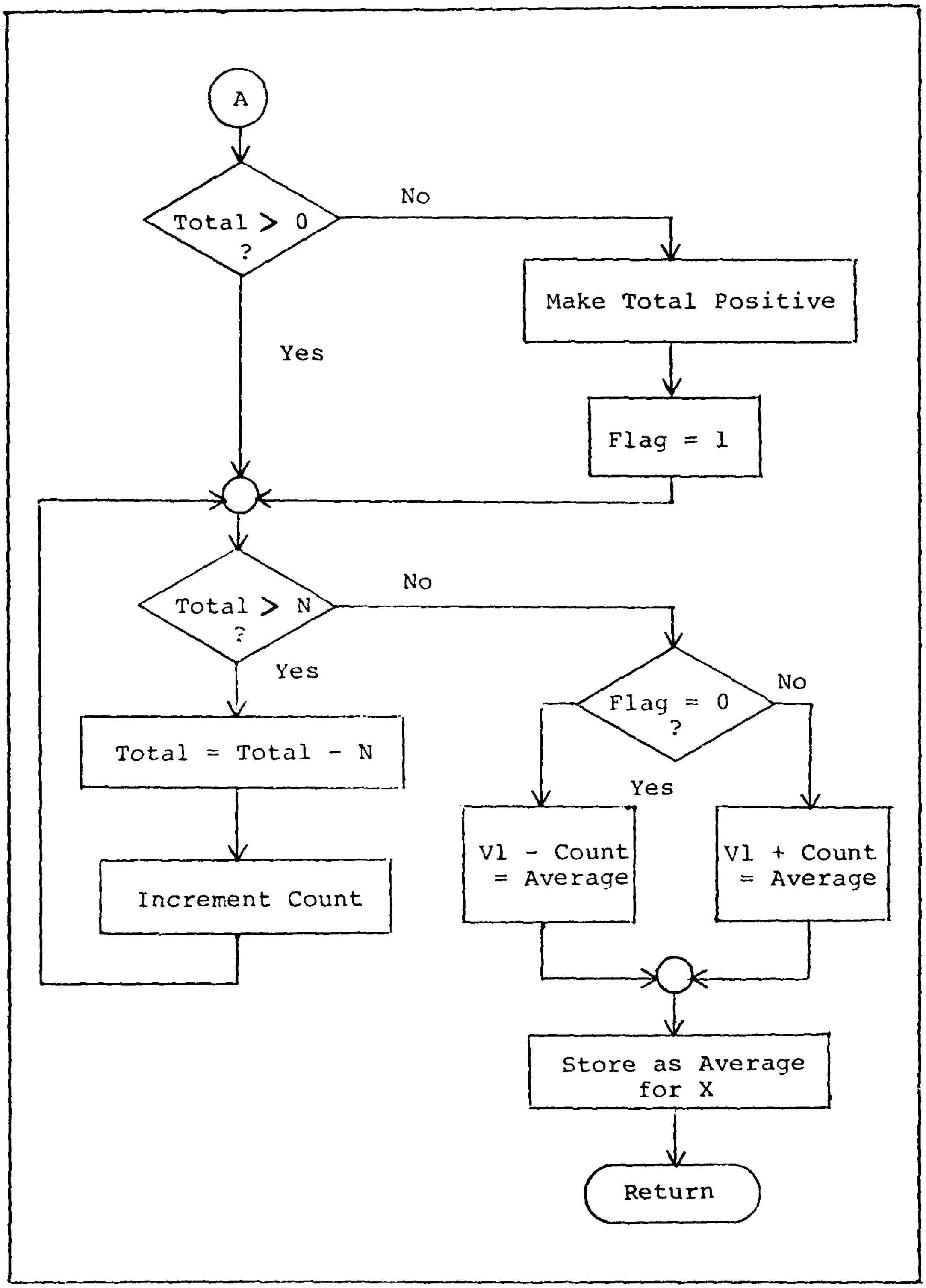


Fig. 20 Average Subroutine Flowchart (Page 2 of 2)

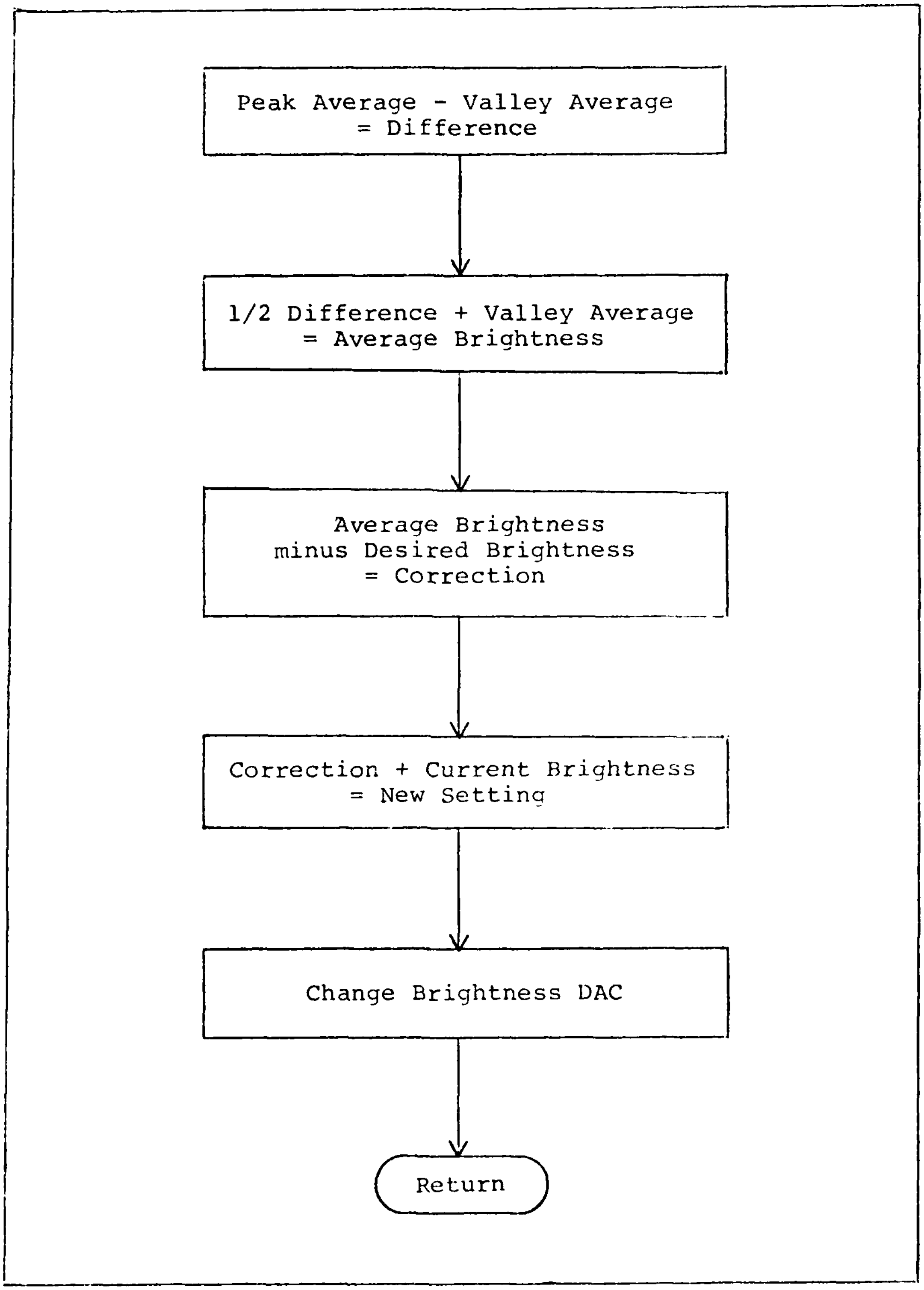


Fig. 21 Brightness Correction Subroutine Flowchart

### Contrast Correction Subroutine

This subroutine (Figure 22) uses the equation, contrast = $\Delta / L_{avg}$, to compute the changes for contrast control. The $\Delta$ is found by:

$$\Delta = \frac{L_{max} - L_{min}}{2} .$$

This $\Delta$ is then used with the current brightness setting ($L_{avg}$) to calculate the contrast. Any difference between the calculated contrast and the desired contrast produces a correction factor. The correction factor is then applied to the current contrast setting to obtain a new setting. Finally, the new setting is sent to the contrast DAC.

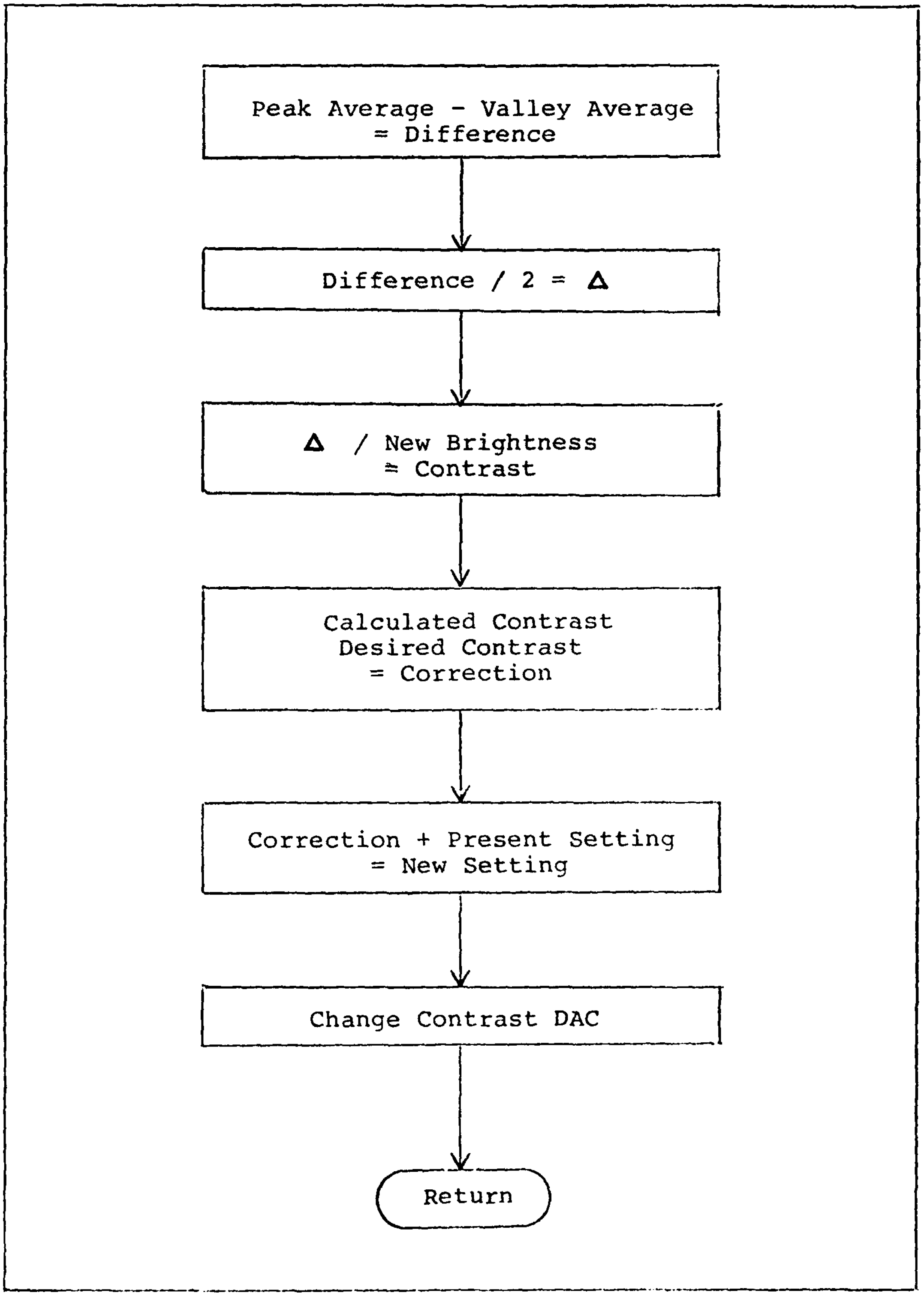


Fig. 22 Contrast Correction Subroutine Flowchart

Appendix C

## Digital Video

This appendix describes another alternative that holds great promise for brightness and contrast control: digitally produced video. A feasibility study was conducted to determine the capabilities of digital video and digitally compatible display devices.

The study revealed that state-of-the-art frame buffers and shadow mask CRTs can provide a grey scale up to 8 bits per picture element (pixel) and resolution of 1024 pixels per line with 900 lines visible. An 8 bit grey scale provides 256 levels of tonal change. This represents a contrast as small as 1/2 of 1%. Another important parameter in vision studies is spatial frequency. The 1024 pixel line produces a spatial frequency of 20 cycles per degree for a subject 2 1/2 feet away from a 19 inch monitor.

Some of the color monitors investigated provided 8 bit resolution on each of the three color guns (red, blue, green). This gives an experimenter amazing flexibility in the choice of color for the visual stimulus. The hi-resolution monitors generally employ dynamic blue-lateral control to improve color registration. The better monitors operate at or above 45 MHz bandwidth. Prices for these monitors run from $15,000 for a 19 inch CRT to $20,000 for a 26 inch CRT. The leading manufacturers in the field are Systems Research Lab and Ramtek.

The majority of the manufacturers providing the memories and circuitry for digital video employ color maps to reduce memory requirements. A color map usually contains 256 colors of 24 bits each (8 bits for each of 3 guns). This allows the individual pixels to be defined by an 8 bit byte. This byte selects 1 of the 256 colors in the color map for presentation on the CRT.

Since 1 byte can be used to define a pixel, a 1024 by 900 buffer needs 900 K bytes of memory. This represents the largest cost in digital video. Complete video systems range in cost from $50,000 to $60,000. An attempt was made to circumvent this expense by designing a custom system for AMRL. The cost in memory parts alone was $40,000, a good indication that the market is not over-priced. Case Western Reserve completed a totally digital picture system in 1977 which cost $400,000 (Ref. 9). However, their system was capable of animation and was controlled by a dedicated PDP-11/45. Today, many manufacturers include interfaces to the standard minicomputers such as the PDP-11 series.

Of the dozen firms examined during the study, Grinnel Systems, Genisco, and Ramtek offer the best digital systems. All three competitors price their 1024 X 1024 X 24 products at approximately $60,000. These prices were the cause of not pursuing this approach beyond the feasibility study.

## Vita

Kenneth L. Martindale was born on 11 November, 1950 in Tulsa, Oklahoma. He graduated from Tulsa Central High School in 1969 and attended the University of Tulsa until 1973 when he received a Bachelor of Science in Electrical Engineering. While attending the University of Tulsa, he participated in the Air Force Reserve Officer Training Program and was commissioned as a second lieutenant in June 1973. After graduation from navigator training at Mather AFB, California, he served as a weapons systems officer in F-4 and F-111 aircraft until May 1979. In June 1979 he was assigned to the Air Force Institute of Technology, Wright-Patterson AFB, Ohio.

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| 20. ABSTRACT (Continue on reverse side if necessary and identify by block number)<br>This report documents the design of a microprocessor based device which controls the brightness and contrast levels of video signals. The device will be used by scientists in vision research to control laboratory monitors.<br>Contrast control in a standard CRT monitor is obtained through the use of a commercial video chip, and brightness control via a straight forward transistor amplifier. The transistor is inserted into the monitor's existing manual control circuit. | | |

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The linear circuit and transistor are regulated by the micro-processor through digital-to-analog converters.

A feedback network reports the actual brightness and contrast produced on the monitor's screen. This network is comprised of a 1024 element photo diode array and an analog-to-digital converter. The photo diode array measures the luminance directly off the monitor and the analog-to-digital converter digitizes the information for use by the microprocessor.

The report also contains the results of an investigation into the use of digitally generated video and color monitors for vision research. The investigation found systems capable of producing 1/2 of 1% contrast, 20 cycles per degree resolution for a subject 2 1/2 feet away, and virtually limitless range of color.

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